



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
PATENT APPLICATION

Applicant : Seong-Hoon Lee  
Application No. : 10/722,959  
Confirmation No. : 9002  
Filed : November 26, 2003  
For : DIGITAL DELAY-LOCKED LOOP CIRCUITS  
WITH HIERARCHICAL DELAY ADJUSTMENT  
Group Art Unit : 2816

New York, New York 10020  
May 5, 2004

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

SUBMISSION OF FORMAL DRAWINGS

Sir:

Pursuant to 37 C.F.R. § 1.85, applicant herewith  
furnishes nine (9) sheets of formal drawings to be  
substituted for the nine (9) sheets of informal drawings  
filed with this application.

Respectfully submitted,

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Signature of Person Signing



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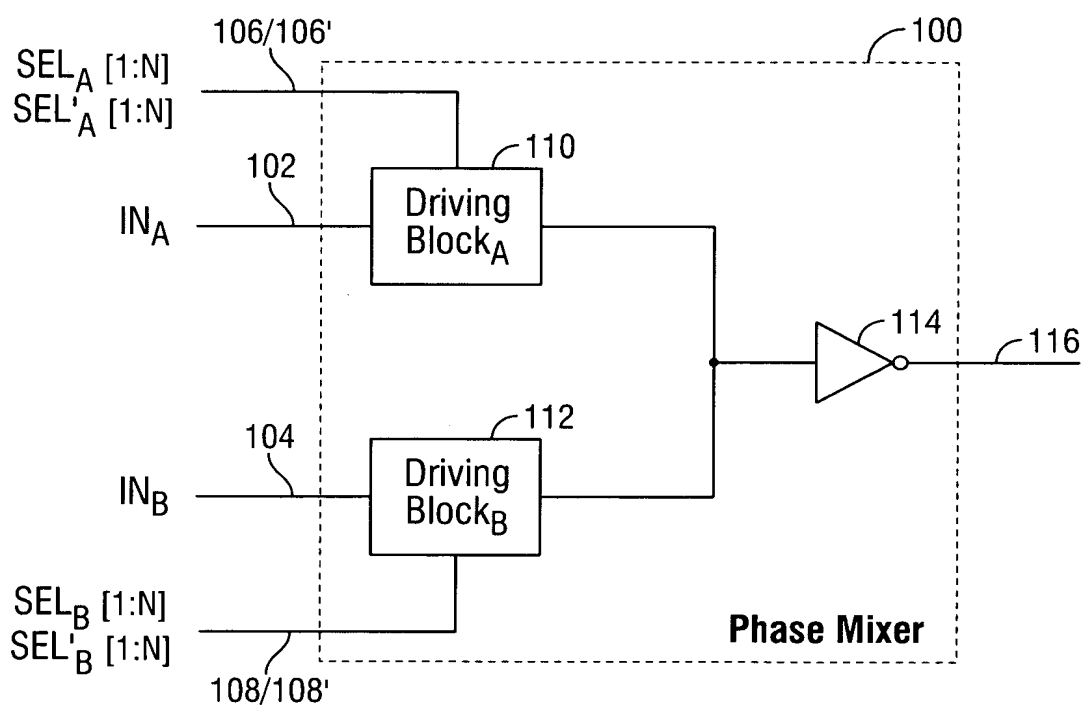


FIG. 1

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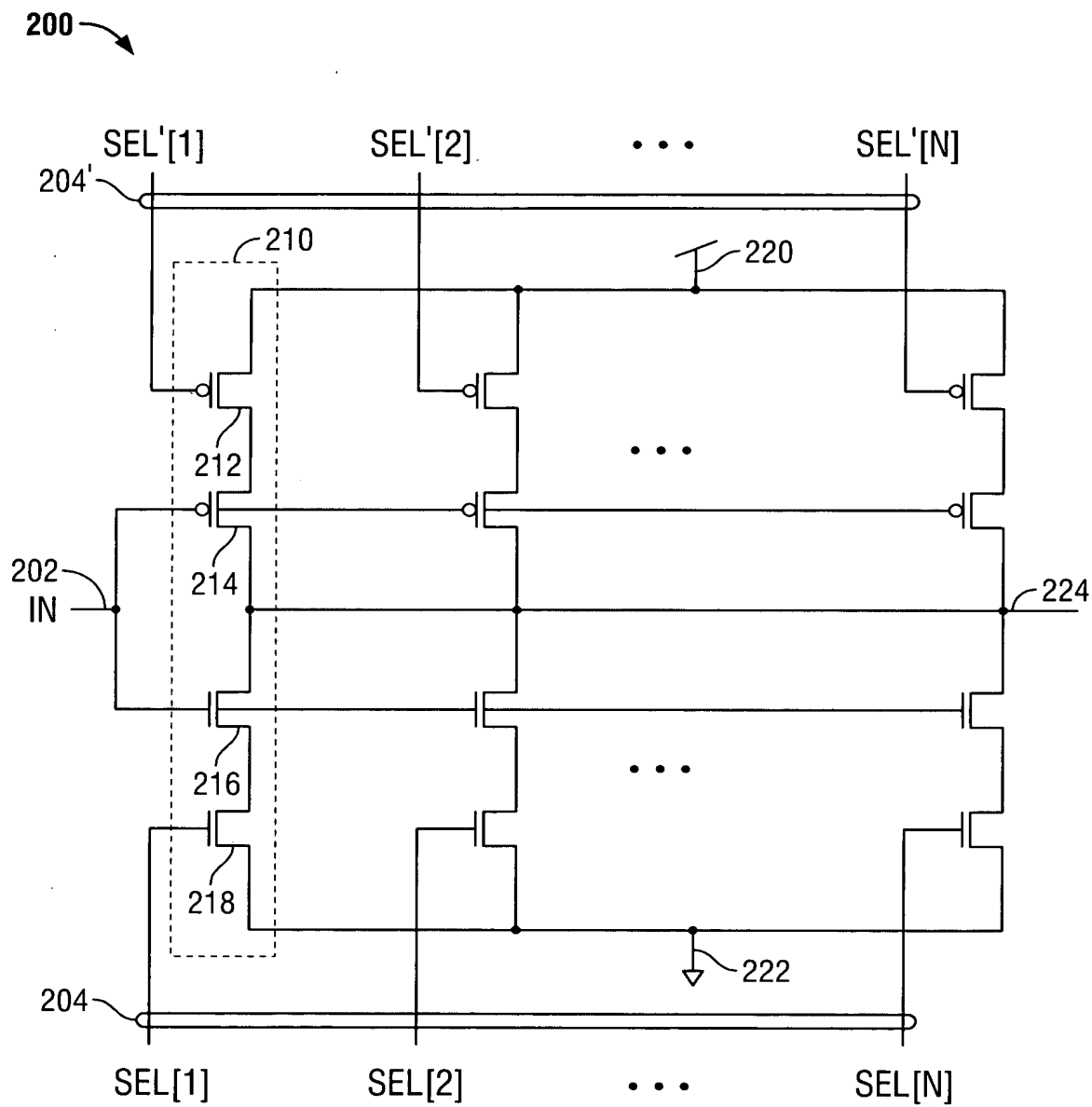
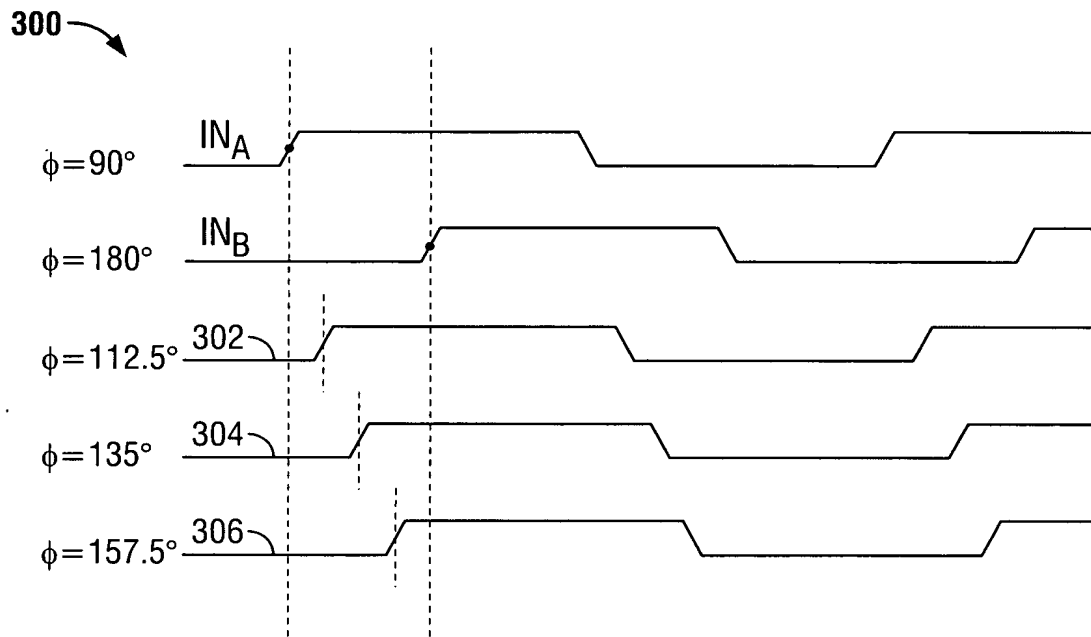


FIG. 2

**3/9****FIG. 3**

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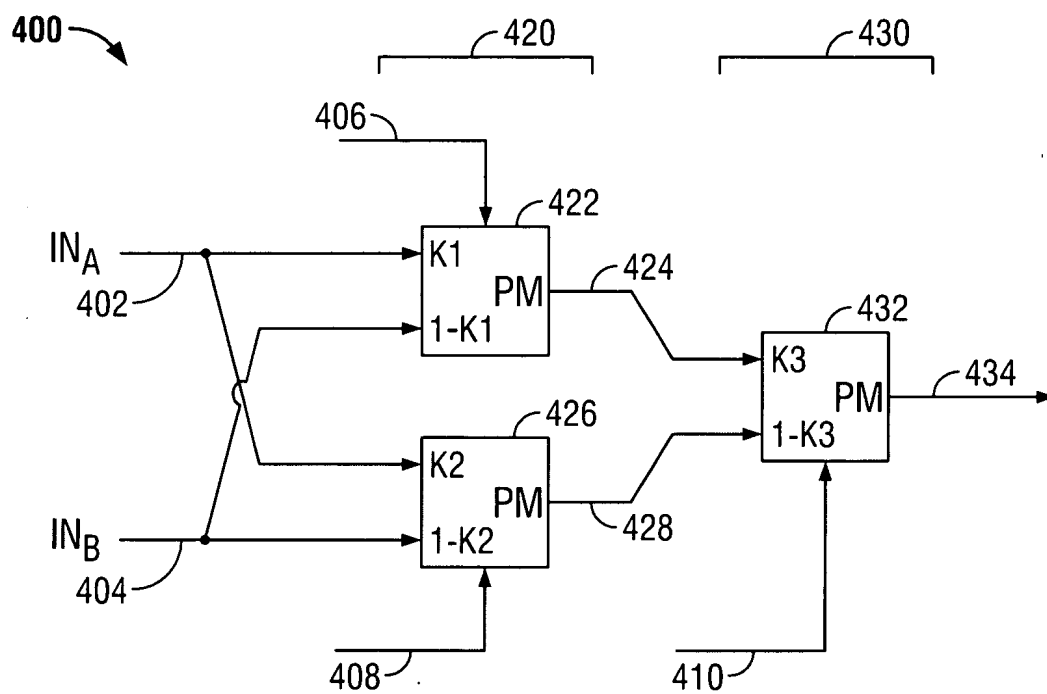
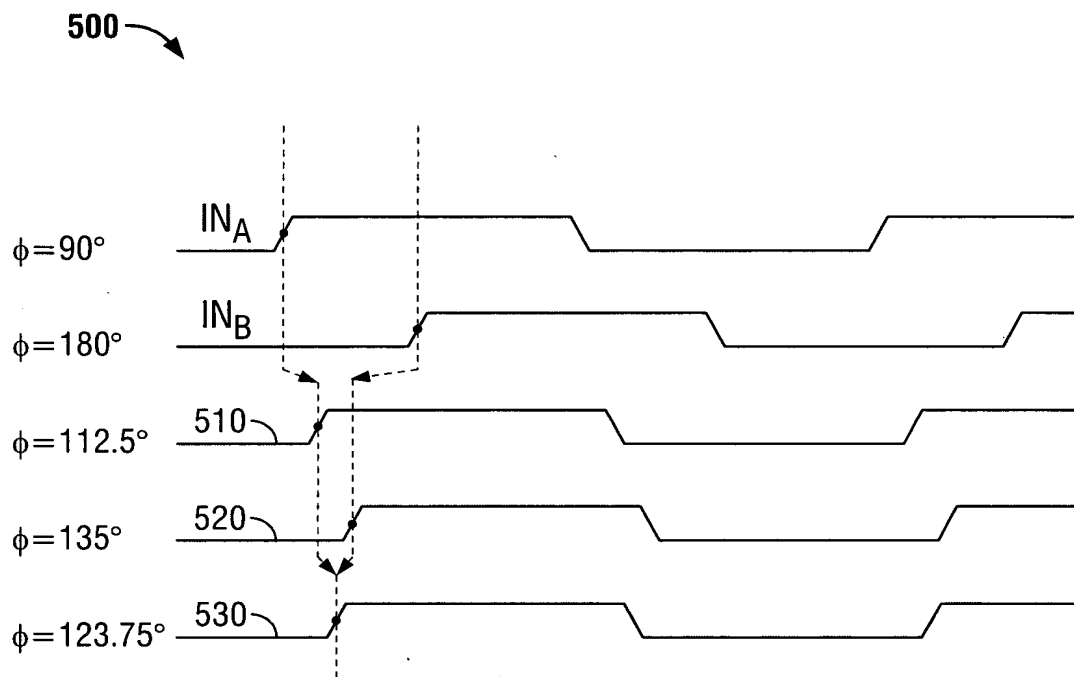


FIG. 4

**5/9****FIG. 5**

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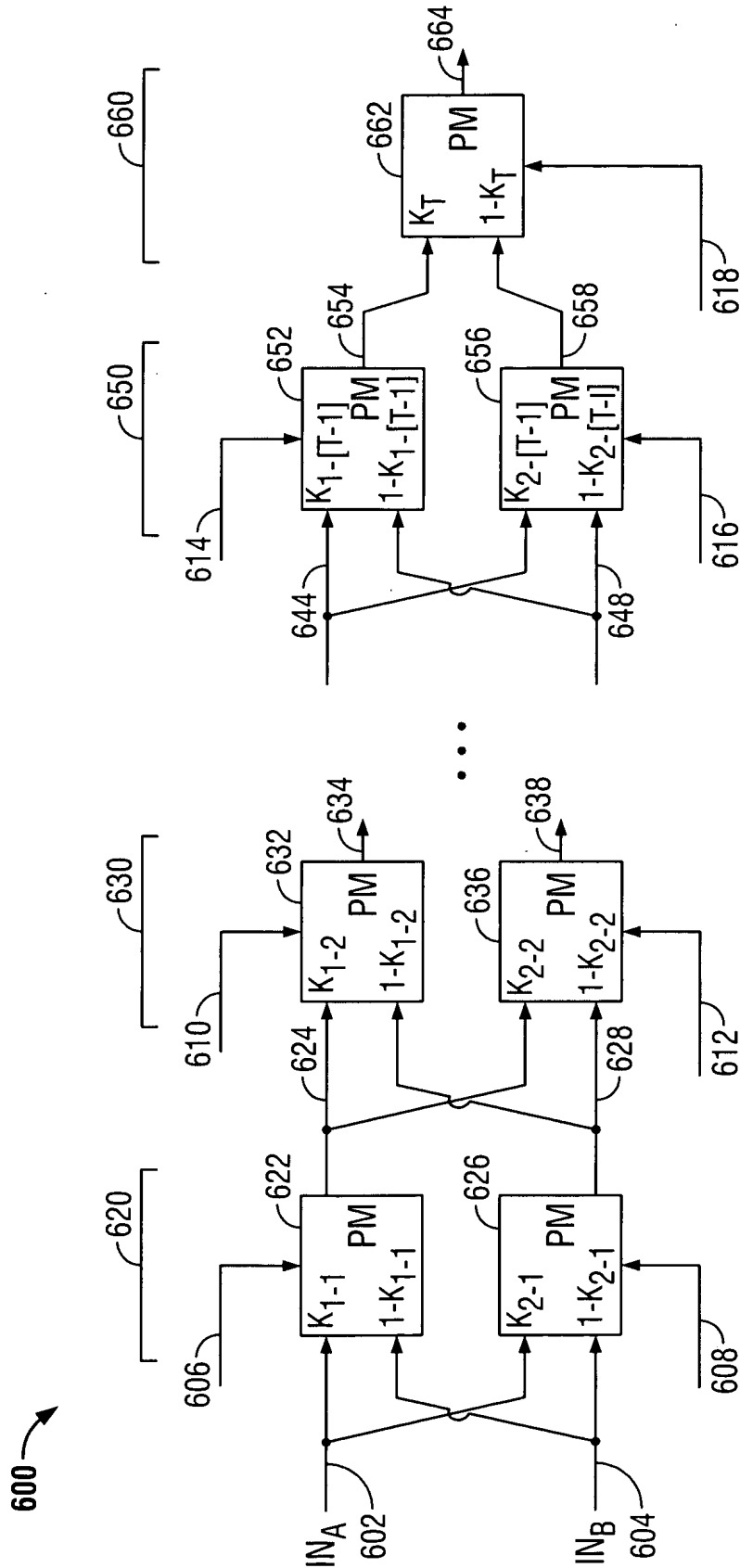


FIG. 6

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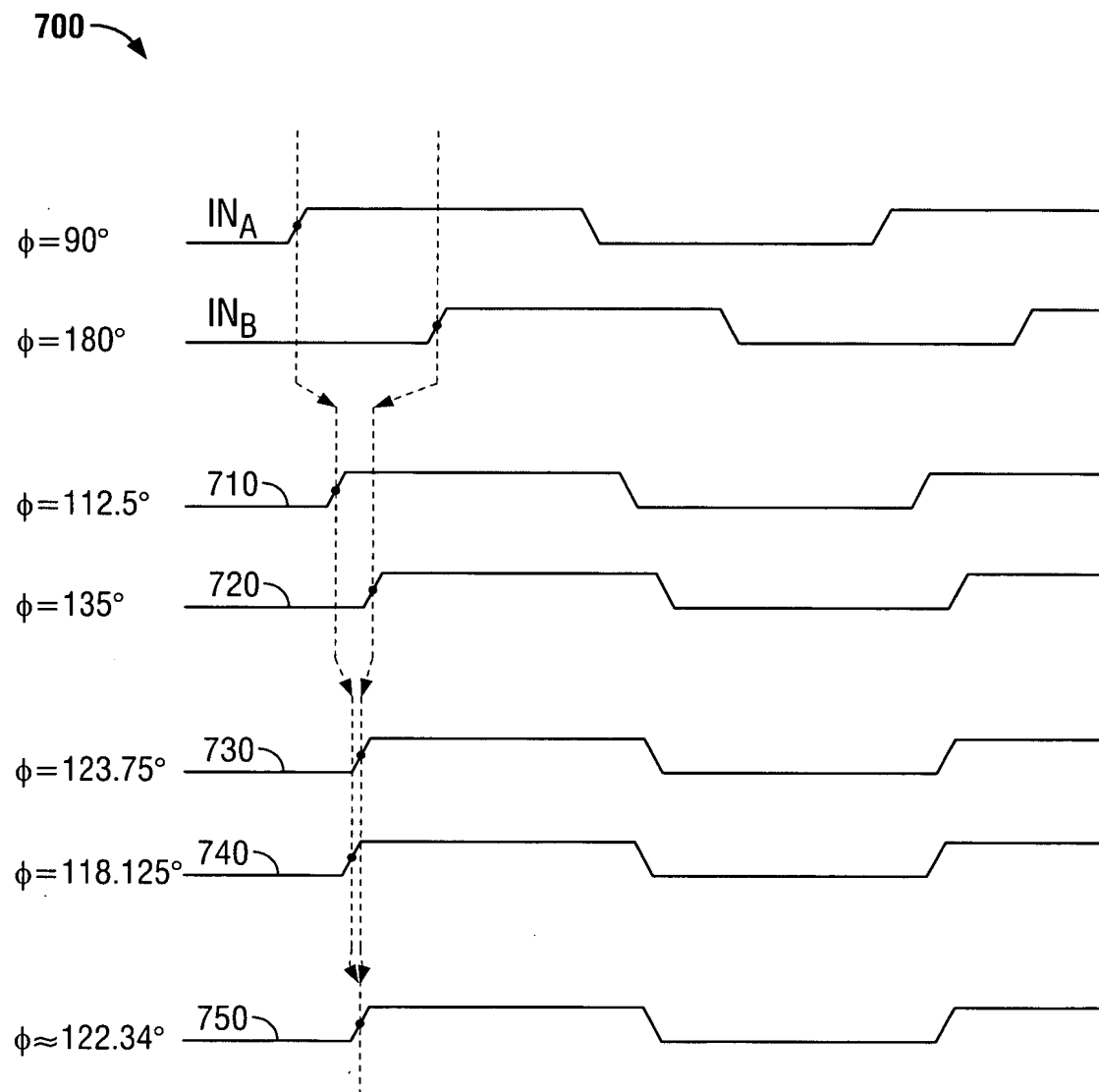


FIG. 7



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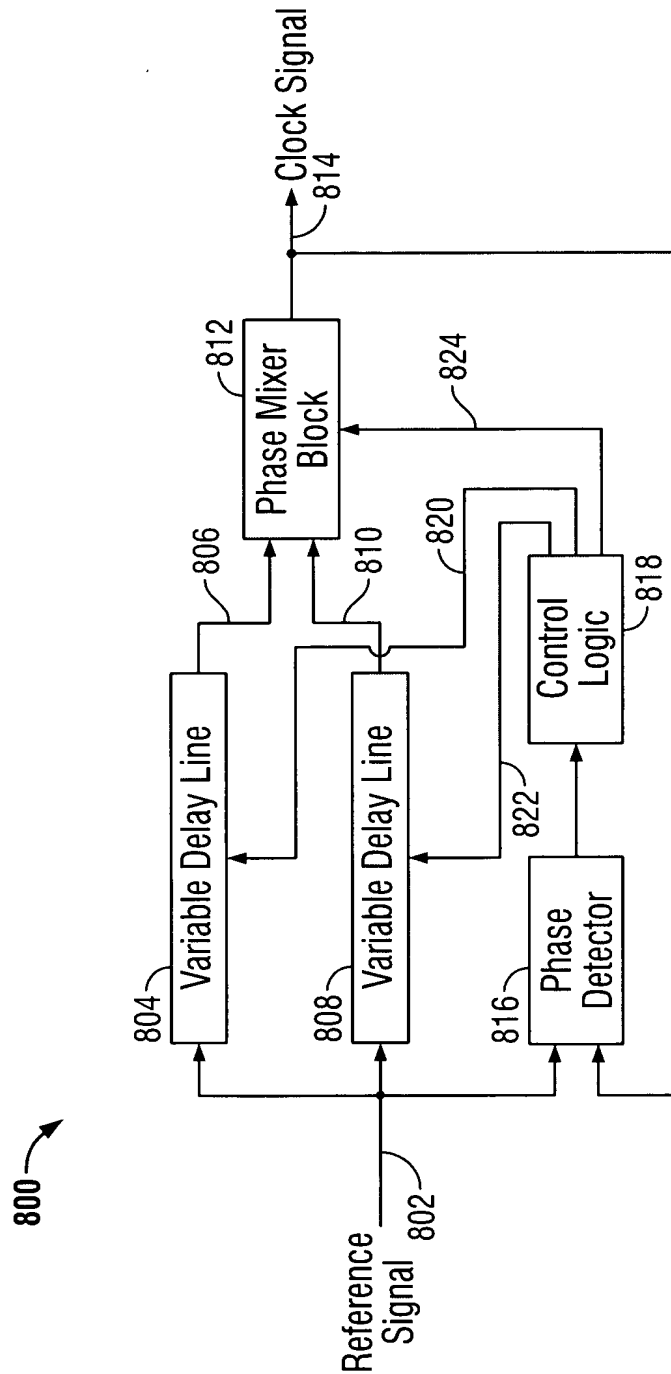


FIG. 8

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